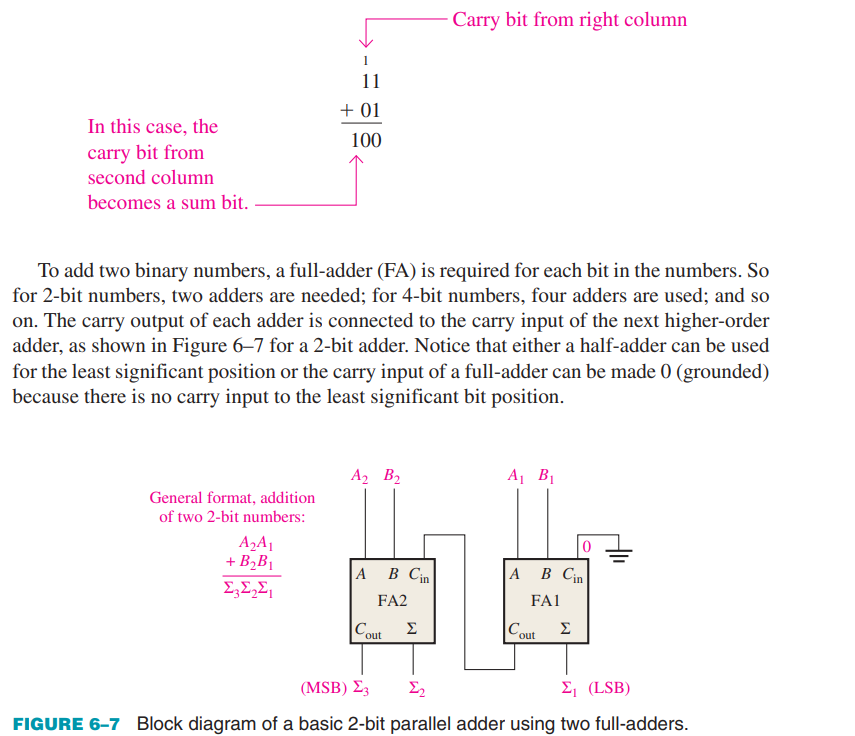
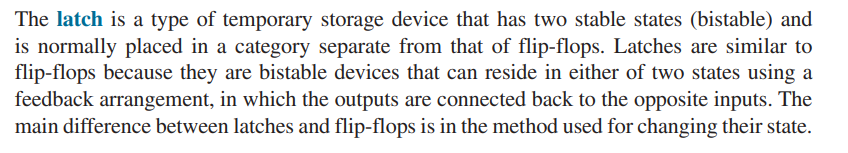
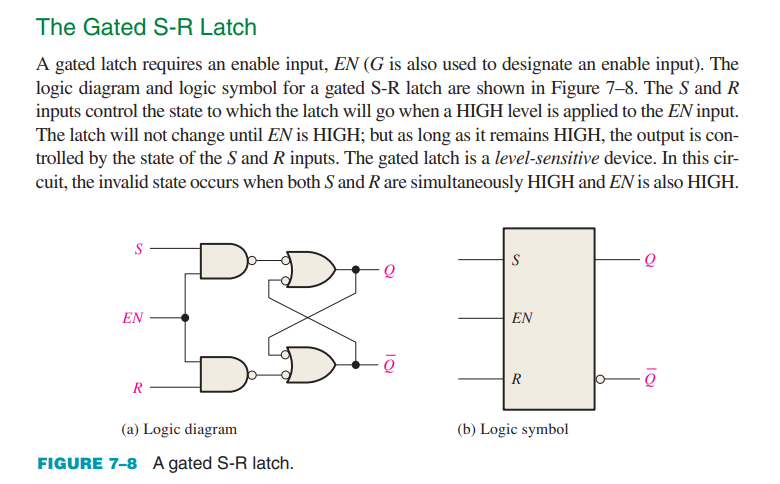
**Parallel Binary Adders:**



Latches:



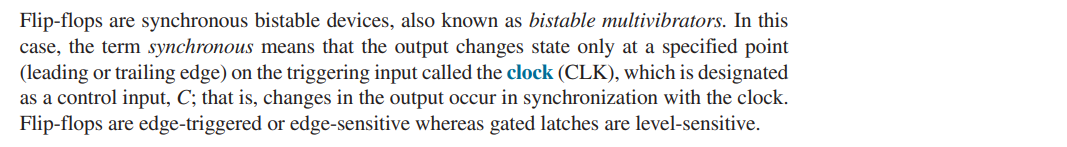
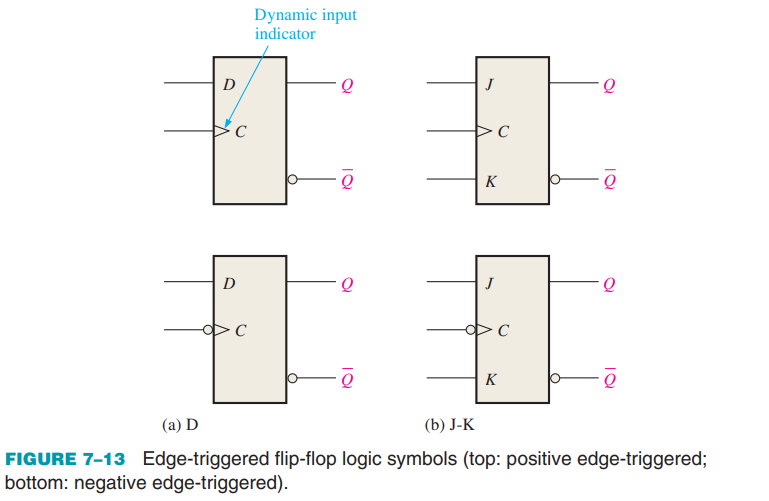
For Simple latches, you will consult youtube, they will be included in quizzes, and finals as well. You must have knowledge of their workings, truth table, timing diagrams etc.



A diagram of a circuit

Description automatically generated

**Flip Flops:**



An edge-triggered flip-flop changes state either at the positive edge (rising edge) or at the negative edge (falling edge) of the clock pulse and is sensitive to its inputs only at this transition of the clock. Two types of edge-triggered flip-flops are covered in this section: D and J-K. The logic symbols for these flip-flops are shown in Figure 7–13. Notice that each type can be either positive edge-triggered (no bubble at C input) or negative edge-triggered (bubble at C input). The key to identifying an edge-triggered flip-flop by its logic symbol is the small triangle inside the block at the clock (C) input. This triangle is called the dynamic input indicator

The dynamic input indicator ­ means the flip-flop changes state only on the edge of a clock pulse.

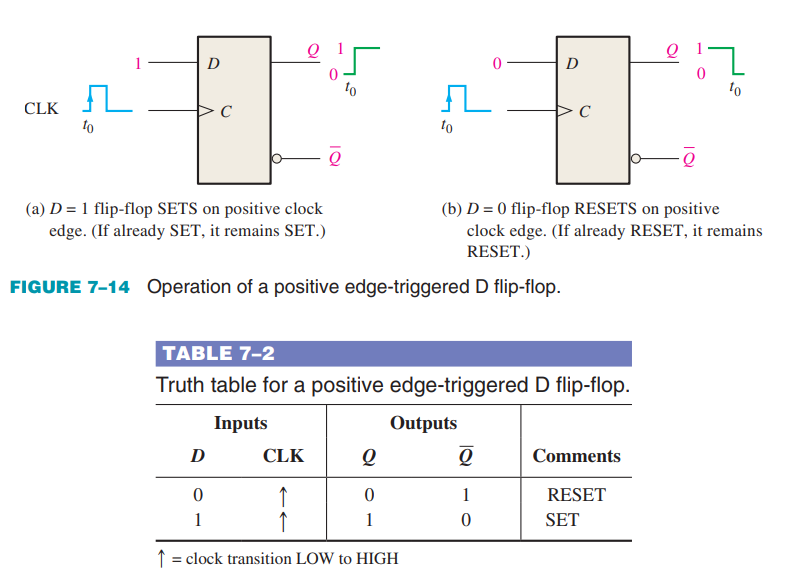
**The D Flip-Flop:**

The D input of the D flip-flop is a synchronous input because data on the input are transferred to the flip-flop’s output only on the triggering edge of the clock pulse.

* When D is HIGH, the Q output goes HIGH on the triggering edge of the clock pulse, and the flip-flop is SET.
* When D is LOW, the Q output goes LOW on the triggering edge of the clock pulse, and the flip-flop is RESET.

This basic operation of a positive edge-triggered D flip-flop is illustrated in Figure 7–14, and Table 7–2 is the truth table for this type of flip-flop. Remember, the flip-flop cannot change state except on the triggering edge of a clock pulse.

The D input can be changed at any time when the clock input is LOW or HIGH (except for a very short interval around the triggering transition of the clock) without affecting the output. **Just remember, Q follows D at the triggering edge of the clock.**

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The operation and truth table for a negative edge-triggered D flip-flop are the same as those for a positive edge-triggered device except that the falling edge of the clock pulse is the triggering edge.

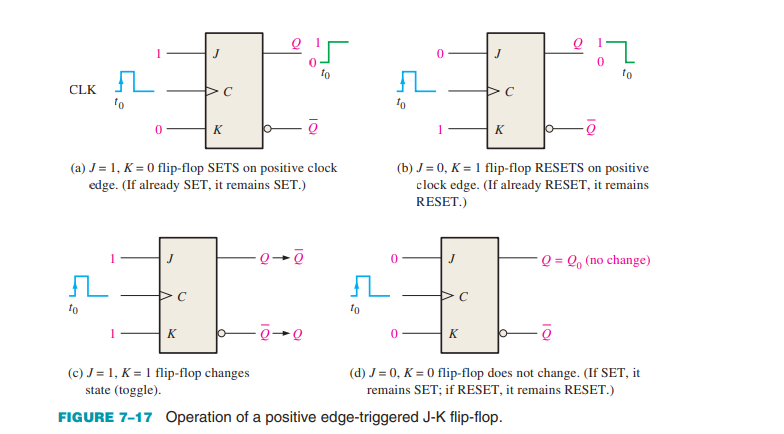
**The J-K Flip-Flop**

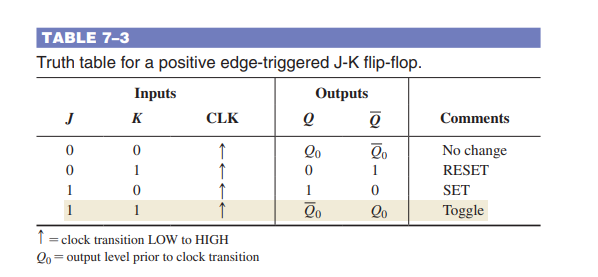
The J and K inputs of the J-K flip-flop are synchronous inputs because data on these inputs are transferred to the flip-flop’s output only on the triggering edge of the clock pulse.

* When J is HIGH and K is LOW, the Q output goes HIGH on the triggering edge of the clock pulse, and the flip-flop is SET.
* When J is LOW and K is HIGH, the Q output goes LOW on the triggering edge of the clock pulse, and the flip-flop is RESET.
* When both J and K are LOW, the output does not change from its prior state.
* When J and K are both HIGH, the flip-flop changes state. This called the toggle mode.

This basic operation of a positive edge-triggered flip-flop is illustrated in Figure 7–17, and Table 7–3 is the truth table for this type of flip-flop. Remember, the flip-flop cannot change state except on the triggering edge of a clock pulse.

The J and K inputs can be changed at any time when the clock input is LOW or HIGH (except for a very short interval around the triggering transition of the clock) without affecting the output.





T Flip Flop:  
Do it yourself. Learn from different sources.

**Registers:**

